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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/756,269	01/09/2001	Niichi Itoh	49657-935	6281

7590 04/06/2005
McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

NGO, CHUONG D

ART UNIT PAPER NUMBER

2193

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/756,269

Applicant(s)

ITOH, NIICHI

Examiner

Chuong D Ngo

Art Unit

2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 6-16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admission of prior art disclosed in figure 18 of the present application in view of in view of Owaki (JP 63055627 A).

As per claims 1-4, the admitted prior art in figure 18 discloses a multiplication apparatus having a Booth encoder (1) Booth selection circuitry (3), intermediate product generating circuitry (4-6) being divided into first array (4a-4d,5a,5b,6a) and second array (4e-4g,5c,5d,6b), and a final addition circuit (7) as claimed. The admitted prior art in figure 18 also discloses the divided arrays arranged in a direction orthogonal to the Booth select control signals, and performing the addition in a direction toward the final addition circuit.

However, the admitted prior art in figure 18 does not show the final addition circuit in between the divided arrays. Nevertheless, 1 Owaki discloses in figure 1, the arrangement of the final addition circuit in between the divided array as claimed for minimizing the wiring delay (see the Constitution, lines 11-12). Thus, it would have been obvious to a person of ordinary skill in the art to arrange of the final addition circuit of the admitted prior art in between the divided array as taught by Owaki in order to minimize the wiring delay, and thus to increase the speed of processing. The arrangement of the final addition circuit of the admitted prior art in between the divided array as taught by Owaki would also result in the transmission of the final intermediate multiplication value from each divided array to said final addition circuit without passing over another divided array as claimed.

As per claim 5, the admitted prior art in figure 18 also does not show the multiplicand generating circuit in between the divided arrays. However, since the multiplicand generating circuit provides a common multiplicand to both the divided arrays, it would have been obvious to a person of ordinary skill in the art to apply the teaching of Owaki as set forth above to arrange the multiplicand generating circuit in between the divided arrays so that the wiring delay can be minimized, and thus further improve the speed of processing.

2. Applicant's arguments filed on 01/26/2005 have been fully considered but they are not persuasive.

It is respectfully submitted that, When placing the final addition circuit of the admitted prior art of figure 8 in between the divided array to minimize the wiring delay as taught by Owaki, the transmission of the final intermediate multiplication value from each divided array to said final addition circuit would not pass over another divided array as claimed.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Tuesday-Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong D Ngo
Primary Examiner
Art Unit 2193

03/29/2005